# Resistive Feedback Influence on Ring Oscillator Performance for IR-UWB Pulse Generator in 0.13µm CMOS technology

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*Abstract* - A CMOS standard three-stage ring oscillator is examined in UMC 0.13µm technologies. As the ring oscillator is a part of IR-UWB (Impulse Radio Ultra Wide Band) pulse generator, its oscillating frequency determines the central frequency of the pulse spectrum and has significant effect on spectrum fitting within UWB FCC mask. The influence of inverter feedback resistors on the ring oscillator frequency and the peak-to-peak amplitude are investigated. Furthermore, as the ring oscillator usually drives a buffer in pulse generator/transmitter chain, dependence of its Figures of Merit on the buffer resistive feedback is presented in the paper.

*Keywords* – CMOS technology, resistive feedback, impulse radio (IR), pulse generator, ring oscillator, ultra-wideband (UWB).

#### I. INTRODUCTION

Impulse Radio Ultra-Wide-Band (IR-UWB) technology has emerged as a potential solution for very high data rate short-range communication, and low data rate communication related to localization, targeting both low cost and low power consumption [1-3]. It transmits extremely short pulses, on the order of a nanosecond or less, which occupy a bandwidth up to several GHz. Additionally, IR-UWB technology offers high fading margin for communication systems in multipath environments [3].

The American Federal Communications Commission (FCC) defines a signal as ultra-wideband if it occupies more than 500 MHz of radio frequency spectrum or exhibits a fractional bandwidth of at least 25% [4]. Since the FCC allocated frequency spectrum for UWB technology is 3.1–10.6 GHz, the power level from the UWB transmitter should be small enough not to interfere with the already existing communication systems such as WiMax, Bluetooth and GSM. This requirement limits output power level of UWB TXs at -41.3 dBm/MHz [4]. In the GPS band (0.96–1.61 GHz), there is even more stringent regulation: less than -75.3 dBm/MHz is needed to

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avoid interference problems. The PSD (Power Spectral Density) in frequency interval from 1.61 GHz to 3.1 GHz depends on the type of application (indoor, outdoor, GPS, wall & medical imaging, through-wall imaging & surveillance system). In spite of these regulations, there have been many reports of interferences with wireless local area network (WLAN) systems operated in the 5–6 GHz band. Therefore, due to practical reasons, the UWB bandwidth is subdivided into two bands: 3–5 GHz (low-band) and 6–10.6 GHz (high-band).

One of the most critical components of an UWB system is the pulse generator, which has to be low power and low complexity. Additionally, spectrum of generated pulse train has to satisfy the FCC spectral mask, making pulse generator design very challenging. There are several typical techniques for designing it which usually follow all-digital [5], [6], analogue/digital [7] or all-analogue [7], [8] design approach. Digital solutions offer higher integration, lower consumption and better controllability while all-analogue techniques demonstrate circuit simplicity.

As an essential part of analogue/digital pulse generator [5], a ring oscillator is studied in this work. Dependence of its performance on inverter and buffer resistive feedbacks is examined in 0.13µm UMC CMOS technology.

# II. STANDARD THREE-STAGE RING OSCILLATOR DESIGN

The pulse generator represents a key block in impulse UWB communications. As pulse shape determines the spectrum characteristic of the UWB signal and effectively dictates specific system requirements, its generation is one of the essential considerations in the UWB design. Fig. 1



Fig. 1. A IR-UWB transmitter based on ring oscillator as a part of pulse generator.



Fig. 2. The three-stage ring oscillator architecture.

shows the basic topology of an IR-UWB transmitter based on ring-oscillator as a part of the pulse generator. It consists of a glitch generator, a switched ring oscillator, a buffer stage and a pulse shaping (band-pass) filter [7]. The glitch generator turns the ring oscillator on/off. It defines ring oscillation time and the width of the pulse. Since the time domain pulse width decides its frequency spectrum [8], it is important to design a pulse, which makes optimal usage of the available spectrum, within the limits imposed by FCC. The switched ring oscillator should generate signal in glitch-defined interval. Its oscillating frequency defines position of the transmitted pulse spectrum within the FCC mask [8]. The buffer isolates the ring oscillator from the pulse shaping filter loading and improves the pulse generator current driving capability. The band-pass filter additionally accommodates the pulse in the allowed spectral mask of FCC.

The switched ring oscillator topology is shown in Fig. 2. It is composed of the three-stage ring oscillator  $(M_1-M_3)$  and a pair of oscillation-enabling switches  $(M_4$  and  $M_5)$ . Due to its simplicity and short start-up time, the ring oscillator is the mostly used architecture in IR-UWB transmitter applications. It has small resistance at each feedback nod which allows fast transient response.

The oscillation-enabling switches, as their name says, control the oscillation process. When the on-off signal (produced by glitch generator) is high,  $M_4$  is turned on ( $M_5$  is turned off), the inverters  $M_1$ – $M_3$  outputs have voltage values determined by the size ratio of the corresponding pMOS and nMOS transistors. Due to the small inverter reactance, the oscillation can start immediately.  $M_5$  turns on ( $M_4$  turns off) at the on-off signal low edge, connecting the  $M_1$  transistor output and the  $M_2$  transistor input to  $V_{dd}$ , and effectively shutting down the oscillation.

# III. RING OSCILLATOR PERFORMANCE

The design proposed have been simulated in mixed mode/RF UMC 0.13 $\mu$ m CMOS eight-metal technology using SpectreRF Simulator from Cadence Design System. Supply voltage V<sub>dd</sub> of this technology is 1.2 V.

The ring working frequency depends directly on transistors sizes. If the transistors are larger, the period of the oscillation *T* rises proportionally, while the oscillating frequency decreases ( $f_0=1/T$ ), and vice versa. For the

NMOS and PMOS ring transistors size, channel width/length: W/L=0.36µm/0.12µm (and identical sizes of all NMOS and PMOS transistors gates), the oscillation frequency of 7.65 GHz has been obtained. It should be noted that this is the smallest NMOS transistor size. The PMOS transistor width (W) could be decreased to 0.32 $\mu$ m, but in inverter topology PMOS transistor is usually equal or two times larger than NMOS transistor. The latter ratio of transistors sizes has been used in buffer stages. To utilize the UWB high-band more effectively, the center frequency of at least 8GHz is required. Higher ring oscillator frequency could be achieved without PMOS transistor M<sub>5</sub>. However, this transistor provides start of the oscillation from the same initial state by connecting A' (B) node to V<sub>dd.</sub> This happens at falling edge the on-off signal, when the oscillation-enabling switch (transistor M<sub>4</sub>) turns off effectively shutting down the oscillations.

#### A. Influence of the inverter resistive feedback

To increase the oscillation frequency at a given DC current, the resistive feedback is used in each inverter stage as proposed in Ref [7]. Resistors are connected between nodes A–A', B–B', and C–C', shown in Fig. 3. Dependence of the ring oscillator performance on the resistor R value is shown in Fig. 4. It can be noticed that with resistor value decrease, oscillation frequency rises,



Fig. 3. The three-stage ring oscillator architecture.



Fig. 4. Dependence of the ring oscillator performance on the inverter feedback resistor value.



Fig. 5. Dependence of the ring oscillator frequency and the peakto-peak amplitude V<sub>pp</sub> on the feedback resistor value.

 TABLE I

 Ring oscillator performance dependence on the inverter

 Resistive feedback

$\mathbf{R}\left(\mathbf{k}\Omega\right)$	f <sub>0</sub> (GHz)	Vpp (mV)
10	8.2	733
8	8.6	690
6	9.1	618
4	9.8	440

while the peak-to-peak amplitude  $V_{\rm pp}$  of the ring output signal reduces as expected, Fig. 5. This is caused by the reduction of the inverter gain with decreasing the feedback resistor value. Furthermore, the  $V_{pp}$  parameter and the time for reaching the peak signal values reduce resulting in the ring oscillator frequency increase. Simulated  $V_{pp}$  and  $f_0$ values of the ring oscillator in 0.18µm technology are presented in Tables I. For R changes from 10 k $\Omega$  to 4 k $\Omega$ , the oscillating frequency is in the range from 8.1 GHz to 9.05 GHz, while  $V_{pp}$  decreases from 733 mV to 440 mV. It can be noticed that the oscillation frequency was changed in the considerably wide frequency range of 1.6 GHz, and the lowest value of 8.2 GHz (obtained for the highest resistor value) is by far larger than 7.65 GHz achieved with standard topology shown in Fig.2. However, the oscillator output amplitude for the lowest resistor value is not large enough to drive properly the subsequent stage (usually a buffer) in the pulse generator chain. Therefore the resistor value should be selected considering the trade-off between the oscillation frequency and the required value for  $V_{pp}$ .

#### B. Influence of the buffer resistive feedback

The method of increasing the ring oscillator frequency by using the inverter resistive feedback is already known in literature, Ref [7]. To the best of our knowledge, the influence of the buffer feedback resistor on the ring performance is still not examined. Fig. 6a shows schematic of the buffer with resistive feedback. To provide better isolation between the ring oscillator and the pulse shaping filter, a two stage buffer is proposed, Fig. 6b. The first stage role is to increase the ring oscillator frequency, while



Fig. 6. Buffer topologies: a) Buffer stage with the resistive feedback b) Two-stage buffer.



Fig. 7. Dependence of the ring oscillator performance on the buffer feedback resistor value.

TABLE II
RING OSCILLATOR PERFORMANCE DEPENDENCE ON THE BUFFER
RESISTIVE FEEDBACK

$\mathbf{R}\left(\mathbf{k}\Omega\right)$	f (GHz)	Vpp (mV)
10	8.1	854
8	8.15	841
6	8.3	820
4	8.5	785
2.32*	9.05	720
$0.8^{**}$	9.8	536

\*Minimal resistance value for the RNHR resistor model. \*Different kind of the resistor model, RNPP0.

the second buffer stage prevents this effect to change the output bandpass filter shaping. Dependence of the ring oscillator performance on the (first) buffer resistive feedback is shown in Fig. 7. Obtained simulation results are summarized in Tables II. Varying *R* from 10 k $\Omega$  to 800  $\Omega$ , the oscillation frequency is increased from 8.1 GHz to 9.8 GHz, followed with decrease in  $V_{pp}$  from 854 mV to 536 mV. As the smallest value of the RNHR high-sheet resistor model is 2.32 k $\Omega$ , the RNPPO UMC resistor model had to be used for 800  $\Omega$ . This value was chosen as it gives the highest frequency value obtained by previous technique. It can be noticed that the available frequency range are increased to 1.7 GHz at the same time with higher  $V_{pp}$  parameter values and larger interval of resistance change. Influence of the buffer resistive

feedback on the ring oscillator can be explained by load changing. The three-stage ring oscillator period T is determined by the propagation time of a signal transition through the complete oscillator chain and is defined as:

$$T = 6 \cdot t_P, \tag{1}$$

where  $t_P$  is propagation delay of the gate. An inverter signal propagation time is largely determined by the strength of the driving gate, and the load presented by the output node itself, which sums the contributions of the connecting gates and the wiring parasitic. Change in the buffer feedback resistor modifies the buffer input impedance (based on Miller's theorem) changing simultaneously the ring oscillator load. This leads to propagation time, and consequently the ring oscillator period/frequency change.

# **III. DISCUSSION**

From the results presented in previous section can be seen that the ring oscillator frequency is strongly dependent on the resistive feedback. The change of the oscillating frequency is 20.9 % for the inverter feedback resistor in the range from 10 k $\Omega$  to 4 k $\Omega,$  and 22.2 % for the buffer feedback and R in the range from  $10 \text{ k}\Omega$  to  $0.8 \text{ k}\Omega$ . Additionally, the maximum frequency (9.8 GHz) obtained by using feedback is remarkably (28.1 %) higher than value (7.65 GHz) achieved without any feedback. Furthermore, simulation results indicate that the peak-to-peak amplitude values of the second method are notably higher comparing to the  $V_{pp}$  values of the first technique obtained for the same oscillating frequency. This can be attributed to the fact that the resistive feedback of the inverter changes directly its gain (and thus the total ring oscillator gain) and currents available to charge/discharge the load capacitance resulting in significant change of voltage peak values. Taking into account the main aim of IR-UWB transmitter design, which includes satisfying the FCC mask requirements with as higher as possible the peak-to-peak amplitude, it could be concluded that the second method gives better ring oscillator performance. Moreover, the maximum frequency of 9.8 GHz and higher  $V_{\rm pp}$  parameter value has been obtained by using only one resistor of 800  $\Omega$  compared with three additional resistors of 4 k $\Omega$ used in the ring resistive feedback. In the field of IC design, it is well known that passive components require considerable die area, increasing the cost and causing problem for area constrained applications. Therefore, from the fabrication cost point of view, the design with buffer feedback will be cheaper.

# **IV. CONCLUSION**

Standard three-stage ring oscillator topology has been analyzed in  $0.13\mu m$  UMC CMOS technology. Dependence of its performance on the resistive feedback of the ring

inverters and the buffer stage has been investigated. Simulations confirmed strong dependency of the ring oscillator frequency and the peak-to-peak amplitude (especially in the case of the ring inverters feedback) on the feedback resistor value. Additionally, the maximum oscillating frequency obtained in both topologies, is significantly higher (28.1 %) compared to the standard ring working frequency. Likewise, simulation results showed better Figures of Merits of the ring oscillator as a part of UWB-IR pulse generator, in case the buffer resistive feedback has been used. In the latter architecture, a two-stage buffer should be used to provide better isolation between the ring oscillator and the pulse shaping filter.

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# References

- M. Ghavami, L. B. Michael, and R. Kohno, "Ultra Wideband Signals and Systems in Communications Engineering," John Wiley&Sons Ltd, 2004.
- [2] K. Siwiak and D. McKeown, "Ultra-Wideband Radio Technology," John Wiley&Sons Ltd, 2004.
- [3] J. R. Fernandes and D. Wentzloff, "Recent Andvances in IR-UWB Transceivers: An Overview," *IEEE Int. Conf. on Circuits and Systems*, pp. 3284–3287, 2010.
- [4] First Report and Order: Revision of Part 15 of the Commission's Rules Regarding Ultra-Wideband Transmission Systems Federal Communications Commission (FCC), ET Docket 98-153, Adopted February 14, 2002, Released Apr. 22, 2002.
- [5] V. V. Kulkarni, M. Muqsith, K. Niitsu, H. Ishikuro, T. Kuroda, "A 750 Mb/s, 12 pJ/b, 6-to-10 GHz CMOS IR-UWB transmitter with embedded on-chip antenna", *IEEE Jour. of Solid. State Circuits*, vol. 44, no. 2, pp. 394-403, Feb. 2009.
- [6] H. Kim, Y. Joo, S. Jung, "A tunable CMOS UWB pulse generator", *The 2006 IEEE International Conference* on Ultra-Wideband, Waltham, MA, pp. 109-112, 24-27 Sept. 2006.
- [7] S. Sim, D.W. Kim, S. Hong "A CMOS UWB pulse generator for 6–10 GHz applications", *IEEE Microwave and wireless components letters*, vol. 19, no. 2, pp. 83-85, Feb. 2009.
- [8] O. Novak, C. Charles, "Low-power UWB pulse generators for biomedical implants", *IEEE International Conference on Ultra-Wideband*, Vancouver, BC, pp. 778-782, 9-11 Sept. 2009.